UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/760,599 | 01/20/2004 | Stephen R. Van Doren | 200313613-1 | 1105 |

22879 7590 01/31/2008

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

| EXAMINER | |
|---|---|
| CHERY, MARDOCHEE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2188 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 01/31/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
mkraft@hp.com
ipa.mail@hp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov



**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/760,599
Filing Date: January 20, 2004
Appellant(s): VAN DOREN ET AL.

Gary J Pitzer
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed November 30, 2007 appealing from the Office action mailed March 21, 2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

10/760,640; 10/760,652; 10/760,659; 10/760,813; 10/761,073.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 2003/0217236 | Rowlands | 2002 |
| 6,138,218 | Arimilli | 2000 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 9, 14, 16-17, 20, 23-24, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Glasco (2005/0251626).

As per claim 1, Glasco discloses a system comprising: a first node that includes an ordering point for data [par. 45, ll 1-3], the first node being operative to employ a write-back transaction associated with writing data back to memory [par. 116, ll 5-8], the first node broadcasting a message to at least one other node in the system in response to an acknowledgement provided by the memory indicating that the ordering point for

the data has migrated from the first node to the memory [par. 87, ll 11-16; pars. 120-123].

As per claim 2, Glasco discloses the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the plurality of cache lines having an associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction [par. 126].

As per claim 3, Glasco discloses the at least one other node provides a response to the first node acknowledging receipt of the write-back message broadcast by the first node [par. 126].

As per claim 4, Glasco discloses the first node maintains the write-back transaction active until the first node receives responses from the at least one other node to the write-back message broadcast by the first node [pars. 121-123, par. 127, ll 13-15].

As per claim 9, the rationale in the rejection of claims 1 and 2 is herein incorporated.

As per claim 14, Glasco discloses the first processor comprises a cache line that contains the desired data in a state that defines the cache line as the ordering point for

the desired data prior to issuing the write-back request to the memory [par. 87, ll 11-16; pars. 120-123].

As per claim 16, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 17, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 20, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 23, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 24, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 2 is herein incorporated.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6, 10-11, 13, 15, 18-19, 21-22, 25-28, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco (2005/0251626) in view of Rowlands (2003/0217236).

As per claim 5, Glasco discloses a third node that issues a source broadcast request for the data employing a source broadcast protocol [par. 127].

However, Glasco does not specifically teach the third node retrying the source broadcast request for the data in response to recognizing a conflict associated with the source broadcast request for the data as required.

Rowlands discloses the third node retrying the source broadcast request for the data in response to recognizing a conflict associated with the source broadcast request for the data [pars. 57 and 113] to write back a remote cache block that is being evicted from the node (par. 65).

Since the technology for implementing a system with a third node retrying the source broadcast request for the data in response to recognizing a conflict associated with the source broadcast request for the data was well known as evidenced by Rowlands, an artisan would have been motivated to implement this feature in the system of Glasco in order to write back a remote cache block that is being evicted from the node. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Glasco to include a third node retrying the source broadcast request for the data in response to recognizing a conflict

associated with the source broadcast request for the data because this would have facilitated writing back a remote cache block that is being evicted from the node (par. 65) as taught by Rowlands.

As per claim 6, Glasco discloses the conflict is recognized by the third node in response to one of (i) receiving the write-back message broadcast by the first node while the source-broadcast request for the data is active at the third node, or (ii) receiving a conflict response from the first node to the source broadcast request issued by the third node [par. 127].

As per claim 10, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 11, the rationale in the rejection of claim 6 is herein incorporated.

As per claim 13, the rationale in the rejection of claim 9 is herein incorporated.

As per claim 15, Glasco discloses the state that defines the cache line as the ordering point for the desired data is selected from a group consisting of a modified state, an owner state and a dirty state, the cache line transitioning to an invalid state after issuing the write-back request to the memory [par. 87, ll 11-16; par. 120].

As per claim 18, Rowlands discloses means for retiring an outstanding transaction associated with migration of the ordering point to the memory from the associated cache in response to receiving the acknowledgment of receipt of source broadcast write-back message [pars. 0057, 0064, 0065, and 113].

As per claim 19, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 21, the rationale in the rejection of claim 15 is herein incorporated.

As per claim 22, the rationale in the rejection of claim 15 is herein incorporated.

As per claims 25 and 26, the rationale in the rejection of claims 5 and 18 is herein incorporated.

As per claim 27, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 28, the rationale in the rejection of claim 6 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 15 is herein incorporated.

Claims 7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco (2005/0251626) in view of Rowlands (2003/0217236) and further in view of Arimilli (6,138,218).

As per claim 7, Glasco and Rowlands disclose the claimed invention as discussed above.

However, Glasco and Rowlands do not specifically teach a third node retries the source broadcast request employing a forward progress protocol as required.

Arimilli discloses a third node retries the source broadcast request employing a forward progress protocol [col. 1, ll 6-12] in order to allow other traffic to proceed and alleviate the prospect of a livelock (col. 1, ll 13-14).

Since the technology for implementing a system with a third node retries the source broadcast request employing a forward progress protocol was well known as evidenced by Arimilli, an artisan would have been motivated to implement this feature in the system of Glasco and Rowlands in order to allow other traffic to proceed and alleviate the prospect of a livelock. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant, to modify the system of Glasco and Rowlands to include a third node retrying the source broadcast request employing a forward progress protocol since this would have allowed other traffic to proceed and alleviated the prospect of a livelock (col. 1, ll 13-14) as taught by Arimilli.

As per claim 12, the rationale in the rejection of claim 7 is herein incorporated.

***Allowable Subject Matter***

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**(10) Response to Argument**

Appellant's argument on page 16 of the remarks that Glasco does not disclose that "an ordering point can migrate from a node to memory and any serialization point for a memory line can migrate", recited in claim 1, is clearly erroneous.

Examiner strongly disagrees with such contention. Examiner would like to first make it clear that though the prior art must disclose the claimed invention in as complete detail as is contained in the claims, this is not however an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Though the prior art may use terms similar to that of applicants' claimed invention, it also suffices that the prior art discloses the claimed subject matter at least in the manner recited in applicants' specification.

As described on page 6, paragraph [0028] of applicant's specification, "the state of a cache line can be utilized to define a cache ordering point in a

system. In particular, for a protocol implementing the states set forth in Table 1 (I, S, E, F, D, M, O), a cache line having one of the states M, O, E, F, or D can serve as an ordering point for the data contained in that cache line. In particular, a cache line having any one of the states M, O, and D ***must*** implement a write-back to memory upon displacement of the associated data. As a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data".

Glasco unequivocally discloses as detailed on page 3 of the Office action mailed on October 6, 2006, and at least in paragraphs [0087, 0091] and paragraphs [0116, 0120-0123], "a system having a cache coherency directory where cache lines have states including modified (M), owned (O), shared (S), dirty (D), and invalid (I). If the directory entry indicates that the line is in the "dirty" state, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" line in a remote cache requires that the remote cache writes the line back to memory". Thus, it is manifest that Glasco discloses, as claimed by applicants, "an ordering point can migrate from a node to memory" by virtue of his disclosure of a cache line having either a modified (M), Owned (O), or dirty (D) state and a write-back to memory upon displacement (i.e., line is dirty or evicted) and consequently a cache ordering point for a given cache line migrates from the cache to memory".

Appellant further submits on page 17, paragraph 1 of the remarks that "the Final Action is attempting to impermissibly use the particular implementation details of the system disclosed in the present application to reject claim 1 and that the present Application (and particularly not paragraph [0028] of the present application) does not qualify as prior under 35 U.S.C 102(e) to support an anticipation rejection of claim 1."

It should be emphasized that the specification was not used in rejecting the claims, rather the combination of Glasco, Rowlands, and Arimilli. Additionally, embodiments of the invention, provided in applicant's specification, are best suitable for a reasonable interpretation of the claimed subject matter.

Examiner would like to make it clear that during examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, 367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004). During examination, the Examiner must give claims their broadest reasonable interpretation (in light of the specification). This means that the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef

America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

Additionally, reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim. The Examiner simply applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification. See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

Appellant's argument on page 17, paragraph 2 that "in Glasco, even during an eviction or write transaction, such as during a write back to memory, a given memory controller remains the serialization point for the memory line before, during and after writing back to memory (See Glasco pars. [0137] and [0127]" is clearly erroneous.

Appellant cites to Glasco, paragraphs [0137] and [0127] in support of these allegations. Examiner would like to impugn such contention by pointing

out that Glasco neither in those paragraphs pointed to by applicants nor anywhere else teaches that "a given memory controller remains the serialization point for the memory line before, during and after writing back to memory" as alleged by applicants. Additionally, Examiner would like to debunk such a claim by first pointing out that such claim appears to be mere allegations for there are no literal, grammatical, exegetical, factual, or legal basis, none whatsoever, supporting these allegations.

Appellant's arguments on page 18, that "Glasco does not appear to have any relationship to the ordering point for a cache line", that "the Final Action has impermissibly relied on the present application's specification to support this contention", and that "the Final Action appears to have misconstrued the teachings of Glasco" are clearly erroneous.

Examiner strongly disagrees since Glasco clearly discloses "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the ***dirty (D) state*** in any of the remote caches, the modified memory line to memory ***must first be written back*** to memory before the line is invalidated in each of the remote caches; paragraphs [0116, 0118, 0120]". As shown above, to have migration of an ordering point as disclosed in applicant's specification, paragraph [0028] "a cache line having a

dirty (D) state must implement a write-back to memory upon displacement of the associated data and as a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data".

Glasco's teaching of "sending invalidation messages to each of the remote caches in a cluster system if the directory entry indicates that the line is in the ***dirty state (D)*** and the modified line must be written back to memory" in fact provides acknowledgment indicating that the ordering point has migrated from a node to memory. Additionally, during examination, interpreting the claims as broadly as their terms reasonably allow, in light of the specification, is not impermissible reliance on the application's specification. In re American Academy of Science Tech Center, 367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004). In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004). See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

Appellant's argument on page 19 that Glasco fails to disclose "a cache line having an associated state that defines the cache line as an ordering

point for the data prior to employing the write back transaction", recited in claim 2, is clearly erroneous.

Examiner respectfully disagrees with such contention. Glasco clearly discloses "if a directory indicates that the line is in a "dirty" state (D) in any of the remote caches, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" (D) line in a remote cache requires that the remote cache write the line back to memory"; pars. [0116, 0120] as permitted by broadest reasonable interpretation in light of applicant's specification at par. [0028] wherein is disclosed "a cache line having any one of the states M, O, and D must implement a write-back to memory upon displacement of the associated data. As a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data". Embodiments of the claimed invention are best suitable in interpreting claims.

Additionally, page 9, paragraph 1 of the remarks filed on December 20, 2006 (though through mischaracterization), attests that Glasco clearly discloses "a cache line having an associated state that defines the cache line as an ordering point for the data prior to employing the write back transaction". In those lines applicant affirms that Glasco teaches in paragraphs [0127] and [0137] "even during an eviction or write

transaction, such as during a write back to memory, a given memory controller remains the serialization point (cache ordering point) of the memory line before, during and after writing back to memory.

Appellant further submits on page 20, paragraph 1 that "the Final Action is attempting to impermissibly use the particular implementation details of the system disclosed in the present application to reject claim 2 and that the present application does not qualify as prior art under 35 U.S.C 102(e) to support an anticipation rejection of claim 2".

As shown above, in regards to claim 1, in the Final Action, "the present application" is not relied upon as a basis for rejection under 35 U.S.C 102 (e) as alleged by appellant, rather the Examiner simply made use of a well known practice of Patent Examination and Prosecution by interpreting the claims as broadly as their terms reasonably allow, in light of "the present specification", which is not impermissible reliance on the application's specification and applicants' disclosed embodiments are best suitable in interpreting the claimed invention. In re American Academy of Science Tech Center, 367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004). In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

Appellant's argument on page 20, paragraph 2 that Glasco fails to disclose that "at least one other node provides a response to the first node acknowledging receipt of the write-back message broadcast by the first node", recited in claim 3, is clearly erroneous.

Examiner strongly disagrees. Contrary to applicants' assumption, Glasco unequivocally discloses "a home controller (one other node) receives the "dirty" copy of the memory line, writes the line back to memory and notifies the cache coherence directory (i.e., the originator of the transaction or first node) that the transaction is complete"; par. [0126].

Appellant further contends on page 21, paragraph 1 that "in Glasco, the originator of the transaction (the cache coherence controller in the home cluster- see Glasco par. [0124]) does not broadcast a write back message"

Glasco clearly disclose that "probe requests are sent to a memory controller that broadcasts probes to various nodes in a system wherein state information associated with various memory lines are used to reduce the number of transactions; par. [0049]. Glasco further discloses that "when the cache

coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry (noting that the data in that location is written back to main memory when that data is evicted from the cache) which corresponds to remotely cached "dirty" memory line, it generates a sized write request specifying no data and directs the request (i.e., broadcast) to the local memory controller corresponding to the memory line, i.e., the home memory controller; par. [0124]."

Additionally, in response to applicant's argument that the references fail to show "the originator (home node) of the transaction does not broadcast a write back message", it is noted that the features upon which applicant relies (i.e., "the originator (home node) of the transaction does not broadcast a write back message") are not recited in the rejected claim(s). The claims simply recite "...***one other node*** broadcasting a write back message..." Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant's argument on page 21, paragraph 2 that "nothing in the cited sections of Glasco or elsewhere in Glasco is there a disclosure that the first node maintains the transaction active until the first node receives responses from at

least one other node to the write back message that was broadcast by the first node" recited in claim 4 is clearly erroneous.

Examiner respectfully disagrees. Glaso clearly discloses "a write back is generated for the cached memory line; the copy of the line in the cache is invalidated and the eviction mechanism is notified when the memory line has been written back to memory; once the memory controller accepts the sized write transaction, it does not allow any further transactions for the same memory line until the eviction process is completed'; pars. [0121-0123, 0127].

Appellant's argument on page 22, paragraph 2 that Glasco does not disclose "a first processor that provides a write back request to transfer an ordering point from cache of the first processor to memory" recited in claim 9, is clearly erroneous.

The response provided above with respect to claim 1 is herein incorporated. Furthermore, Glasco unequivocally discloses as detailed on page 3 of the Office action mailed on October 6, 2006, and at least in paragraphs [0087, 0091] and paragraphs [0116, 0120-0123], "a system having a cache coherency directory where cache lines have ***states including modified (M), owned (O), shared (S), dirty (D), and invalid (I)***. If the directory entry indicates that the line is in the "dirty" (D) state, the modified memory line must first be written back to memory; the eviction of a cache

coherency directory entry corresponding to a "dirty" (D) line in a remote cache requires that the remote cache writes the line back to memory". In Fig. 2 and paragraph [0126], Glasco further discloses [processors 202a-202d performing write backs; instructing a remote processor to write back a specific "dirty" (D) line in its cache to memory]. Thus, it is manifest that Glasco discloses, as claimed by applicants, "processor that provides a write-back request to transfer an ordering point for desired data from associated cache of the first processor to memory" by virtue of his disclosure of a cache line having either a modified (M), Owned (O), or dirty (D) state and a write-back to memory upon displacement (i.e., line is dirty or evicted) and consequently a cache ordering point for a given cache line migrates from the cache to memory".

Appellant's argument on page 23, paragraph 2 that Glasco fails to disclose "an associated state of a cache line defines the cache line as an ordering point for the data" recited in claim 14, is clearly erroneous.

As shown above, particularly, with respect to claim 1, these arguments were fully addressed and Glasco indisputably discloses "an associated state of a cache line defines the cache line as an ordering point for the data" i.e., "if a directory indicates that the line is in a "dirty" state (D) in any of the remote caches, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a

"dirty" (D) line in a remote cache requires that the remote cache write the line back to memory"; pars. [0116, 0120] as permitted by broadest reasonable interpretation in light of applicant's specification at par. [0028] wherein is disclosed "a cache line having any one of the states M, O, and D must implement a write-back to memory upon displacement of the associated data. As a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data".

Appellant's argument on page 24, paragraph 1 that Glasco does not disclose "means for issuing a write-back request to migrate an ordering point for data from an associated cache memory", recited in claim 16, is clearly erroneous.

As shown above, particularly, with respect to claim 1, Glasco unequivocally discloses, as described on page 6, paragraph [0028] of applicant's specification, "the state of a cache line can be utilized to define a cache ordering point in a system; an associated state of a cache line defines the cache line as an ordering point for the data" i.e., "if a directory indicates that the line is in a "dirty" state (D) in any of the remote caches, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" (D) line in a remote cache requires that the remote cache write the line back to memory"; pars. [0116, 0120], where the

means for issuing the write back could be any of cache coherence controller 230 or processors 202a-202d of Fig. 2". Thus, Glasco clearly discloses "means for issuing a write-back request to migrate an ordering point for data from an associated cache memory" as permitted by broadest reasonable interpretation in light of applicant's specification at par. [0028] wherein is disclosed "a cache line having any one of the states M, O, and D must implement a write-back to memory upon displacement of the associated data. As a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data".

Appellant's argument on page 25, paragraph 1, with respect to claim 23, that Glasco fails to disclose "a write-back request from a first processor node is provided to transfer an ordering point to memory" and that there is no basis to conclude that "the originator of the write back (the first processor node) also provides a source broadcast message to other nodes in response to an acknowledgment receipt of the write back request" is clearly erroneous.

As shown above, particularly, with respect to claims 1, 18, 20 and 22, Glasco clearly discloses "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the dirty (D) state

in any of the remote caches, the modified memory line to memory must first be written back to memory before the line is invalidated in each of the remote caches; paragraphs [0116, 0118, 0120]". As shown above, to have migration of an ordering point as disclosed in applicant's specification, paragraph [0028] "a cache line having a dirty (D) state must implement a write-back to memory upon displacement of the associated data and as a result of implementing the write-back, a cache ordering point for a given cache line migrates from the cache of an associated processor to memory so that the memory contains a coherent copy of the data". In Fig. 2 and paragraph [0126], Glasco further discloses [processors 202a-202d performing write backs; instructing a remote processor to write back a specific "dirty" line in its cache to memory].

Glasco further discloses that "probe requests are sent to a memory controller that broadcasts probes to various nodes in a system wherein state information associated with various memory lines are used to reduce the number of transactions; par. [0049]. Glasco further discloses that "when the cache coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry (noting that the data in that location is written back to main memory when that data is evicted from the cache) which corresponds to remotely cached "dirty" memory line, it generates a sized write request specifying no data and directs the request (i.e., broadcast) to the local memory controller

corresponding to the memory line, i.e., the home memory controller; par. [0124]."

Appellant's argument on page 25, paragraph 2, with respect to claim 24, that Glasco fails to disclose "providing a response from each of the other nodes to acknowledge receipt of the source broadcast message at the other nodes" and that "the originator of the transaction does not broadcast a write back message" is clearly erroneous.

As shown above, particularly, with respect to claims 1 and 20, Glasco unequivocally discloses "a home controller (i.e., one other node) receives the "dirty" copy of the memory line, writes the line back to memory and notifies the cache coherence directory (i.e., the originator of the transaction or first node) that the transaction is complete"; par. [0126]. Glasco further discloses that "when the cache coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry (noting that the data in that location is written back to main memory when that data is evicted from the cache) which corresponds to remotely cached "dirty" memory line, it generates a sized write request specifying no data and directs the request (i.e., broadcast) to the local memory controller corresponding to the memory line, i.e., the home memory controller; par. [0124]."

Appellant's argument on page 26, paragraph 2, with respect to claim 29, that Glasco fails to disclose "a processor that comprises cache lines that contains data in a state that defines a cache line as the ordering point for the data prior to issuing the write back request to the memory" is clearly erroneous.

As shown above, particularly, with respect to claims 1 and 22, Glasco clearly discloses "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the dirty (D) state in any of the remote caches, the modified memory line to memory must first be written back to memory before the line is invalidated in each of the remote caches; paragraphs [0116, 0118, 0120]". In Fig. 2 and paragraph [0126], Glasco further discloses [processors 202a-202d performing write backs; instructing a remote processor to write back a specific "dirty" (D) line in its cache to memory].

Appellant's arguments on page 27, last paragraph, with respect to claim 5, that Glasco in view of Rowlands does not teach or suggest that "a transaction would be retried in response to recognizing a conflict", as recited in claim 5.

Examine respectfully disagrees. Glasco clearly discloses "it is possible that conflicting transactions may be generated during the time between when the cache coherence directory to evict a particular entry and the corresponding request is received by the memory controller; par [0137], while Rowlands discloses "retrying an address transfer to permit a modified cache block to be written to memory, or other coherency activity to occur; [par. 0113].

Appellant further submits on page 27, last paragraph, that "Glasco and Rowlands", taken alone or in combination fail to provide sufficient motivation to create the system of claim 5."

Examiner would like emphasize that in determining obviousness under 35 U.S.C 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "By holding that courts and patent examiners should look only to the problem the patentee was trying to solve;" (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem;" (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the conbination of elements was obvious to try;" and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factfinders recourse to common sense."

Furthermore, the Supreme Court stated that: "When a work is available in one field of endeavor, design incentives and other market forces can promp variations of it, either in the same field or a different one. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the court states that "the focus when making a determination of obviousness should be on what a person of ordianry skill in the pertinent art would have known at the time of the invention...and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowlegdge in the art, or common sense".

Finally, for purposes of 35 U.S.C 103, prior art can be either in the field of applicant's endeavor or be reasonably pertinent to the particular problem with which the applicant was concerned. Furthermore, prior art that is in a field of endeavor other than that of the applicant, or solves a problem which is different from that which the applicant was trying to solve, may also be considered for the purposes of 35 U.S.C 103. See, e.g., In re *KSR International Co. v. Teleflex Inc.*, 550 U.S. at_,82 USPQ2d at 1396 (2007).

In this case, the motivation to combine Glasco and Rowlands is found in the prior art itself as shown in the Final Office Action mailed on March 21, 2007.

Appellant's argument on page 28, with respect to claim 6, that Glasco does not teach "a third node can recognize a conflict" is clearly erroneous.

Examiner respectfully disagrees. Claim 6 recites in the alternative "a conflict is recognized by a third node in response to one of (i) receiving a source broadcast write-back request provided by a first node while a source-broadcast request for the desired data is active at the third node, or (ii) receiving a conflict response from a first node to the source broadcast request issued by the third node."

Glasco clearly discloses "it is possible that conflicting transactions may be generated (i.e., recognized by the originator node) during the time between when the cache coherence directory to evict (write back) a particular entry and the corresponding request is received by the memory controller (i.e., third node); par [0137].

Appellant's argument on page 29 that Rowlands fails to teach or suggest that a third node issues a source broadcast request for the desired data and such third node reissues the request in response to recognizing a conflict associated with the source broadcast request for the desired data" with respect to claim 10.

Claim 10 is rejected under 35 U.S.C 103 as being obvious over the combination of Glasco and Rowlands. Glasco discloses that "probe requests are sent to a memory controller that broadcasts probes to various nodes in a system

wherein state information associated with various memory lines are used to reduce the number of transactions; par. [0049]. Glasco further discloses that "when the cache coherence directory associated with the cache coherence controller in a particular cluster, i.e., the home cluster, determines that it needs to evict an entry (noting that the data in that location is written back to main memory when that data is evicted from the cache) which corresponds to remotely cached "dirty" memory line, it generates a sized write request specifying no data and directs the request (i.e., broadcast) to the local memory controller corresponding to the memory line, i.e., the home memory controller; par. [0124]." Glasco clearly discloses "it is possible that conflicting transactions may be generated during the time between when the cache coherence directory to evict a particular entry and the corresponding request is received by the memory controller; par [0137], while Rowlands discloses "retrying (i.e., reissue) an address transfer to permit a modified cache block to be written to memory, or other coherency activity to occur; [par. 0113].

Appellant's arguments on page 29 that "Glasco and Rowlands, taken individually or in combination fail to provide sufficient motivation to create the system of claim 10" is clearly erroneous.

The Supreme Court, in re *KSR International Co. v. Teleflex Inc.,* 550 U.S. at_,82 USPQ2d at 1396 (2007), stated that: "When a work is available in one

field of endeavor, design incentives and other market forces can promp variations of it, either in the same field or a different one. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the court states that "the focus when making a determination of obviousness should be on what a person of ordianry skill in the pertinent art would have known at the time of the invention...and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowlegdge in the art, or common sense". The Examiner recognizes that the suggestion or motivation to combine the references can be found in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Appellant's arguments on page 30 that "Glasco has no teaching or suggestion that any third node can recognize a conflict in response to the conditions recited in claim 11."

Claim 11 recites in the alternative "a conflict is recognized by a third node in response to one of (i) receiving a source broadcast write-back request provided by a first node while a source-broadcast request for the desired data is

active at the third node, or (ii) receiving a conflict response from a first node to the source broadcast request issued by the third node."

Glasco clearly discloses "it is possible that conflicting transactions may be generated (i.e., recognized by the originator node) during the time between when the cache coherence directory to evict (write back) a particular entry and the corresponding request is received by the memory controller (i.e., third node); par [0137].

Appellant's arguments on page 31 that "Glasco fails to teach or suggest that a state of a cache line can define a cache line as an ordering point" recited in claims 15 and 21 are clearly erroneous.

The reasoning presented above in response to claim 1 also applies to claims 15 and 21 and therefore is herein referenced to rebutting appellant's contention that "Glasco fails to teach or suggest that a state of a cache line can define a cache line as an ordering point."

Appellant argues on page 32 that the rejection of claim 18 has been mischaracterized and that claim 18 recites "means for retiring..." instead of "means for retrying".

This simply was a typographical error. Applicant's disclosure states in paragraphs [0060, 0063, 0066] that "upon receiving the XV-ACK responses from all other nodes in the network 200, the node 208 retires the MAF entry 214; in response to receiving the XV-ACK responses from the other nodes, the requestor node 186 retires its MAF entry 190 and remains in the I-state." Rowlands discloses, in a manner similar to that of applicant's disclosure, "the probe commands are responded to (after effecting the state changes requested) using a Kill_Ack; the Kill_Ack command is an acknowledgment that a kill command (i.e., retire the data associated with the probe commands and the receiving and requesting node) has been processed by the receiving node; the Kill command used to request that a remote owner invalidate (i.e., the I-state) a cache blocks; pars. [0064; 0065]". Rowlands further discloses "retrying an address transfer to permit a modified cache block to be written to memory, or other coherency activity to occur; [par. 0113]" where it would have been apparent to one of ordinary skill in the art that the step of "retrying" would not be performed indefinitely and would retire at some point.

Appellant argues on page 33 that Glasco taken in view of Rowlands fails to teach or suggest "means for recognizing a conflict associated with data" recited in claim 19.

Glasco clearly discloses "it is possible that conflicting transactions may be generated (i.e., recognized by the originator node) during the time between when the cache coherence directory to evict (write back) a particular entry and the corresponding request is received by the memory controller (i.e., third node); par [0137], while Rowlands discloses "retrying an address transfer to permit a modified cache block to be written to memory, or other coherency activity to occur; [par. 0113].

Appellant argues on page 34 that the incorporation of the rationale provided in the Final Action is an insufficient basis for the rejection of claims 25 and 26.

Claims 25 and 26 were rejected under 35 U.S.C 103 as being obvious over the combination of Glasco and Rowlands. Rowlands discloses as shown above, in a manner similar to that of applicant's disclosure, "the probe commands are responded to (after effecting the state changes requested) using a Kill_Ack; the Kill_Ack command is an acknowledgment that a kill command (i.e., retire the data associated with the Kill command and the receiving and requesting node) has been processed by the receiving node; the Kill command used to request that a remote owner invalidate a cache blocks; pars. [0064] [0065]."

Appellant argues on page 35, paragraph 1, that Glasco in view of Rowlands fails to teach or suggest any "structure programmed of configured for recognizing a conflict associated with a request for data provided by at least one of the other nodes", recited in claim 27.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., structure programmed of configured for recognizing a conflict associated with a request for data provided by at least one of the other nodes) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant argues on page 35, paragraph 2, that Glasco has no teaching or suggestion that any other node can recognize a conflict in response to the conditions recited in claim 28.

Claim 28 recites, inter alia, in alternative form "recognizing the conflict in response to one of (i) receiving a source broadcast write-back request provided by a first node while the source-broadcast request for the data is outstanding at least at one of the other nodes, or (ii) receiving a conflict response from a first node to the source broadcast request issued by at least one of the other nodes."

Glasco clearly discloses "it is possible that conflicting transactions may be generated (i.e., recognized by the originator node) during the time between when the cache coherence directory to evict (write back) a particular entry and the corresponding request is received by the memory controller (i.e., third node); par [0137].

Appellant argues on page 37 that in Arimilli, the cache 116 that issues the retry 206 does not retry its transaction using any forward progress protocol, but instead it is the responding cache 114 that initiates the action to enable an intervention response to proceed.

Appellant's arguments appear as though the node retrying the source broadcast request is itself the source (i.e., home) node. However, such is not recited in the claims. Claims 7 and 12 simply recite "the third node retries the source broadcast request employing forward progress protocol" where it is worth mentioning that the node retrying the source broadcast request (i.e., third node) is not the source (i.e., home) node. Arimilli discloses "a node retrying snoop operations using forward progress; col. 1, lines 6-12."

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery
Examiner

Conferees:

Hyung Sough
Supervisory Patent Examiner
01/25/08

/Lynne H Browne/
Lynne H. Browne
Appeal Practice Specialist, TQAS
Technology Center 2100